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TITLE: Performance parameters for cell transfer variations and cell transfer timing in ATM Network
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Summary
Network performance in B-ISDN networks depends primarily on the three lower layers of the B-ISDN protocol : the physical layer, the ATM layer and the AAL layer [1,p267]. Network performance parameters for the ATM layer is the most important. And it includes six QoS parameters which used to measure the performance of the network for a given connection such as: cell loss ratio (CLR), maximum cell transfer delay (Max-CTD),peak-to-peak cell delay variation (P2P-CDV), cell error ratio (CER), severely errored cell block ratio (SECBR), cell misinsertion rate (CMR) [2,p16] . This paper focus on analyzing performance parameters for cell transfer variations and cell transfer timing.

1. Introduction

The network performance parameters for the ATM layer are divided into three groups: those for cell errors, those for cell transfer variations and those for cell transfer timing [1,p273].

1.1. Performance parameters for cell errors

The performance parameters defined for cell errors include the cell error rate and the severely errored cell block ratio.

+ Cell Error Ratio (CER)

$$CER = \frac{\text{Errored Cells}}{\text{Successfully Transferred Cells} + \text{Errored Cells}}$$

The cell error rate is the relationship between the number of cells transferred with errors and the sum of these plus the successfully transferred cells. Errored cells in 'severely errored cell blocks' are not counted [3,p546] [1,p273].

+ Severely Errored cell Block Ratio (SECBR)

$$SECBR = \frac{\text{Severely Errored Cell Blocks}}{\text{Total Transmitted Cell Blocks}}$$

The severely errored cell block ratio is the ratio of severely errored cell blocks to the overall block length within a specified time period [1,p273], [3,p546].

1.2. Performance parameters for cell transfer variations

The performance parameters for cell transfer variations include the cell loss ratio and the cell misinsertion rate [1,p273].

+ Cell Loss Ratio (CLR)

$$CLR = \frac{\text{Lost Cells}}{\text{Total Transmitted Cells}}$$

The cell loss ratio is the number of cells lost within a period as a proportion of the total number of cells transferred during this period. Cells transferred or lost within severely errored cell blocks are not counted [1,p273],[3,p547]..

+ Cell Misinserted Rate (CMR)

$$CMR = \frac{\text{Misinserted Cells}}{\text{Time Interval}}$$

The cell misinsertion rate is the number of misinserted cells (cells with an invalid VPI/VCI due to unrecognized header errors) transferred within a specified time period, divided by the time [1,p273],[3,p547]..

1.3. Performance parameters for cell transfer timing

The performance parameters defined under this heading are the mean cell transfer delay and the cell delay variation [1,p274].

+ Mean Cell Transfer Delay (CTD)

The mean cell transfer delay is the arithmetic mean of a specific number of cell transfer delays.

+ Cell Delay Variation (CDV)

There are two distinct types of cell delay variation (CDV): 1-point CDV, 2-point CDV [1,p274].

In this paper, we focus on analyzing and examination of CLR, CTD based on YATS simulator.

2. Problem and Solve

Figure 1: A Multiplexer

Given 3 source input in a Multiplexer (MUX) buffer, they coupled at the UNI into ATM network. Every source has constant bit rate, supply a ATM cell (53 byte) to MUX per 129.276911μs. We suppose that three sources have following rates:

Src[1] has average arrival cell rate 10,000 cell/sec

Src[2] has average arrival cell rate 8,125 cell/sec

Src[3] has average arrival cell rate 5,081 cell/sec

We thus have the arrival rate is:

λ = Src[1] + Src[2] + Src[3]

= 10,000 cell/sec + 8,125 cell/sec + 5,081 cell/sec = 23,206 cell/sec

Input rate is : 23,206 * 53 * 8 = 9,839,344 bit/s ≈ 9.83 Mb/s

An example we make a simulation on computer with its rate is 10Mb/s ≈ 10,485,760 bit/s

So process rate is : μ = 10,485,760 / (53 * 8) = 24,730.57 cell/sec

Line utilization factor is: $\rho = \lambda / \mu$ = 23,206 / 24,730.57 = 0.938

Interarrival time between two cells is:

$$\tau = 3 / 23{,}206 = 1.29276911 * 10^{-4} \text{ sec} = 129.276911\ \mu s$$

Because of using M/D/1 queue in ATM, we have the average number of cells [E(n)] in the MUX [4,p188].

$$E(n) = [\rho/(1-\rho)]*[1-(\rho/2)]$$

$$= [0.938/(1-0.938)]*[1-(0.938/2)] = 8.034 \text{ cell}$$

Average cell process time is

$$E(\tau) = \rho/\lambda = 0.938/23{,}206 = 4.04206 * 10^{-5} \text{ sec} = 40.4206\ \mu s$$

Average waiting time in the queue [5.16] is:

$$E(W) = [\lambda.\ E(\tau^2)]*[2(1-\rho)]$$

We have $E(\tau^2) = \sigma^2 + E^2(\tau)$, but M/D/1 queue have $\sigma^2 = 0$

So $E(\tau^2) = E^2(\tau)$

Replace in E(W), we have : $E(W) = [\lambda.\ E^2(\tau)]*[2(1-\rho)]$

$$E(W) = [23{,}206 * (4.04206 * 10^{-5})^2]*[2(1-0.938)]$$

$$= [379145.4073*10^{-10}]*[0.124] = 47014.0305052*10^{-10} \text{ sec}$$

Thus E(W) is very small, so when the simulator runs, we will see cell loss in MUX is 0.

3. Simulation results

3.1. Overview of YATS

YATS (Yet Another Tiny Simulator) is a small discrete-time simulation tool tailored for investigation of ATM networks. YATS provides elements of ATM network such as different cell sources, multiplexers, demultiplexers, delay lines and measurement devices etc…It also supports graphical online displays [6,p1].

The system uses a simple script language for the problem description, and is written itself in C++.

Additionally, measurement devices with graphical online displays can be defined. These objects ask network objects for exporting addresses of variables to be displayed, and process and display the values on their own. This ensure that the complexity of network objects is independent on the possibilities for measurement and online display.

3.2. simulation results

The simulation is associated with Linux shell programming using YATS. Linux shell programming supports of creating the simulation's interface. This simulation provides some options which present the simulation capability of YATS. This simulation consits of 7 options. Each option relates to some elements of ATM network as well as their parameters. We can make the input file in several ways by using YATS features (Figure 2).

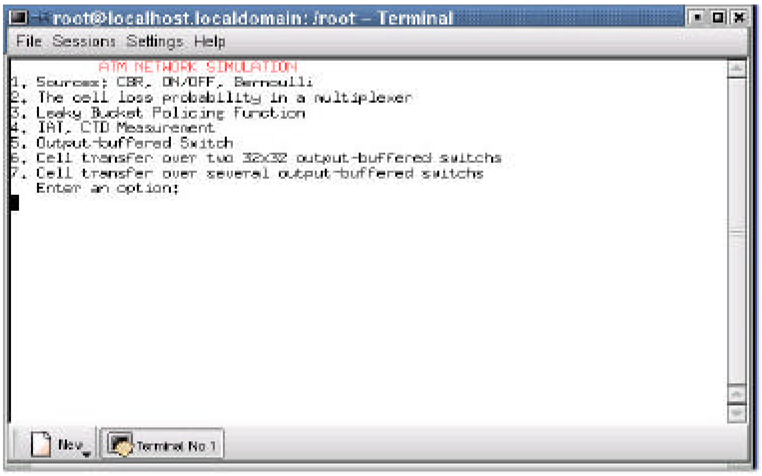

Figure 2: The first simulation interface

1) Simulation Sources:

We simulate cell transfering and measure total cell sent, total cell loss and cell loss rate. In Figure 3, we show the 3 source input given in a multiplexer buffer as following rate: Each Src[1], Src[2], Src[3] of the input source in1, in2, in3 has arrival cell rate 10,000 , 8,125 , 5,081 cell/sec. After simulate the model, we got zero cell loss as the results. In this case, each input has different sources such as CBR, Bernoulli, ON/OFF. During the queue length window expressed running of cells, we can monitor the amount of cells after running. According to the screen, "full x: 20000 slots" means 20000 cells, "last x: slot 99900" means last display cell is 99900th cell, "full y: 100" means average amplitude units and "last y: 10" means amplitude of last cell after running (right side) is 10 units.

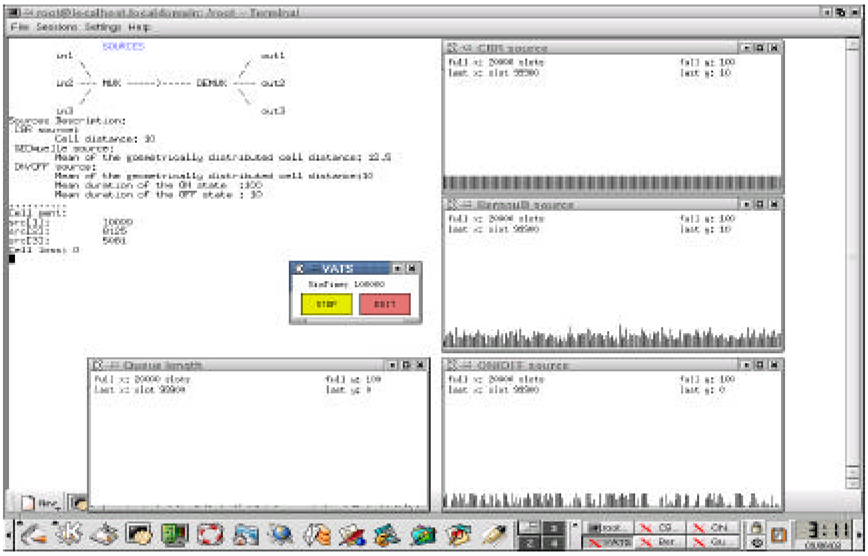

Figure 3: Transfering some cell sources

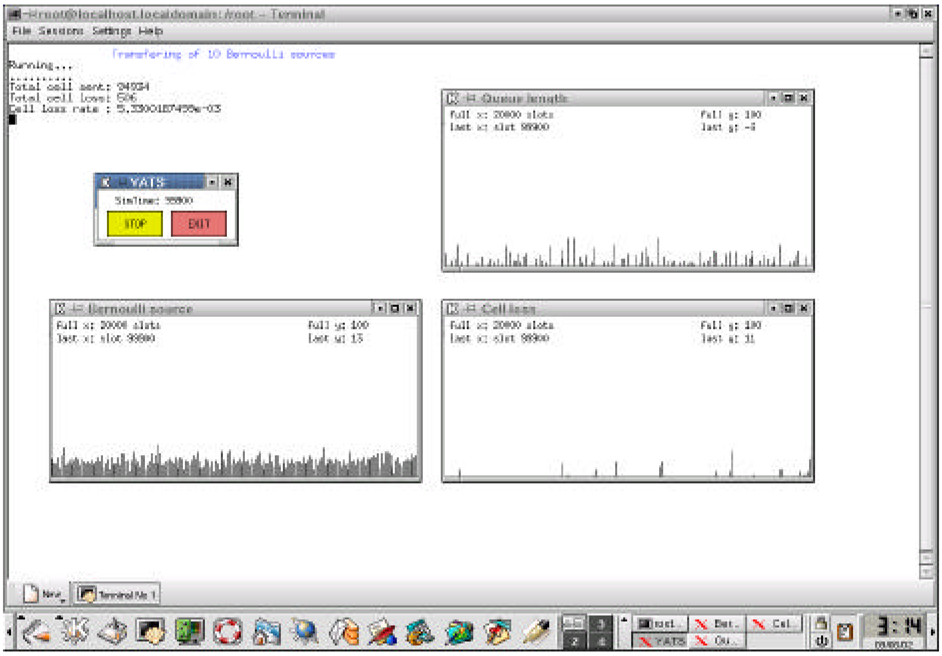

Figure 4 : Transfering Bernoullil source

In Figure 4, we show 10 Bernoulli sources input in a multiplexer buffer. We have 94934 total cell sent and we got 506 total cell loss.

2) Cell loss probability

We simulate the effect of buffer size to the cell loss probability. In Figure 5, we display the cell loss probability in a multiplexer (horizontal axis: buffer length, vertical axis: cell loss probability). As a result, when the buffer length is 100, it shows the minimum of cell loss probability.

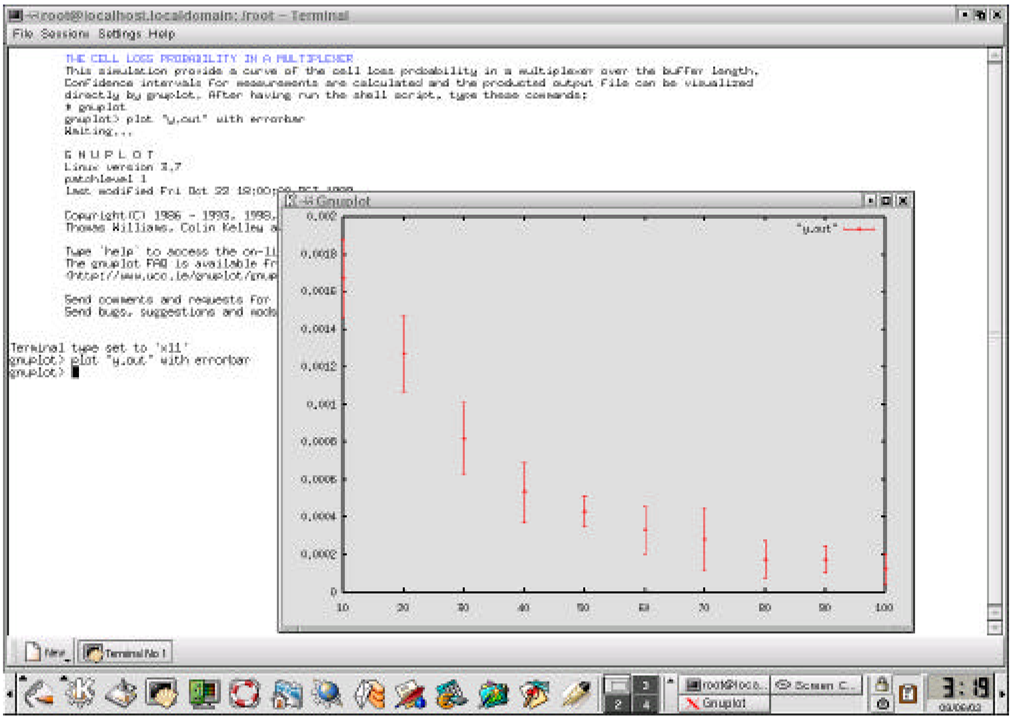

Figure 5 : The effect of buffer size to the cell loss probability

3) Leaky Bucket Policing

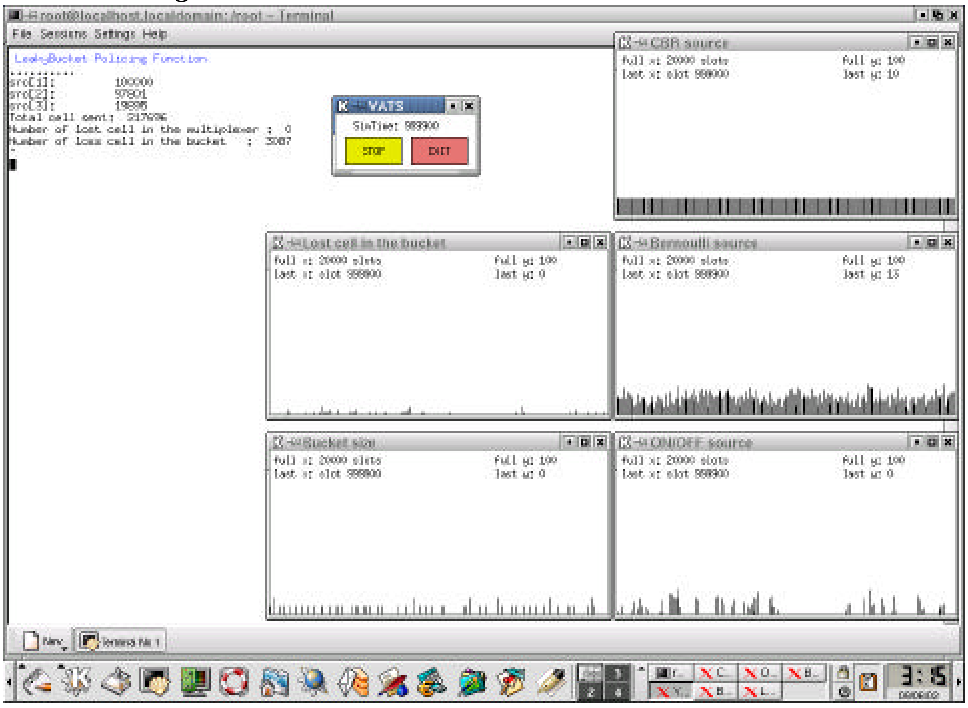

Figure 6 : Leaky Bucket Policing Function

In Figure 6, we expressed that if given 3 source input in a multiplexer buffer are Src[1] : 100000, src[2]: 97801, src[3]: 19895, we have total cell sent : 217696 under control of leaky bucket policing . We got the zero lost cells in the multiplexer but we got 3087 loss cell in the bucket.

4) Cell Transfer Delay Measurement

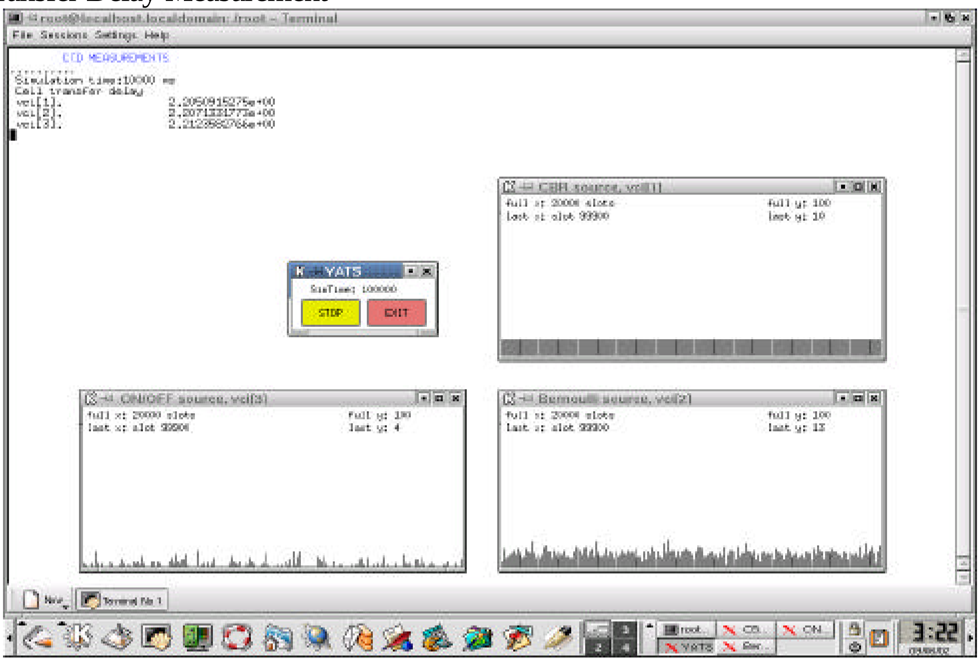

Figure 7: Cell transfer delay measurement

In Figure 7, if we suppose 3 source input in a multiplexer buffer like model in Figure 3, we got the cell transfer delay with the simulation results such as: vci[1] is 2.2050915275e+00; vci[2] is 2.2071331773e+00; vci[3] is 2.2123582766e+00.

5) Cell transfer over an switch

In Figure 8, we examined cell transfer over an switch , we got cell loss and cell passed the switch on each output 1 to output 16 listed result on this figure while we enter the dimention of the switch is 16 (that means 16 x 16 output buffered switch).

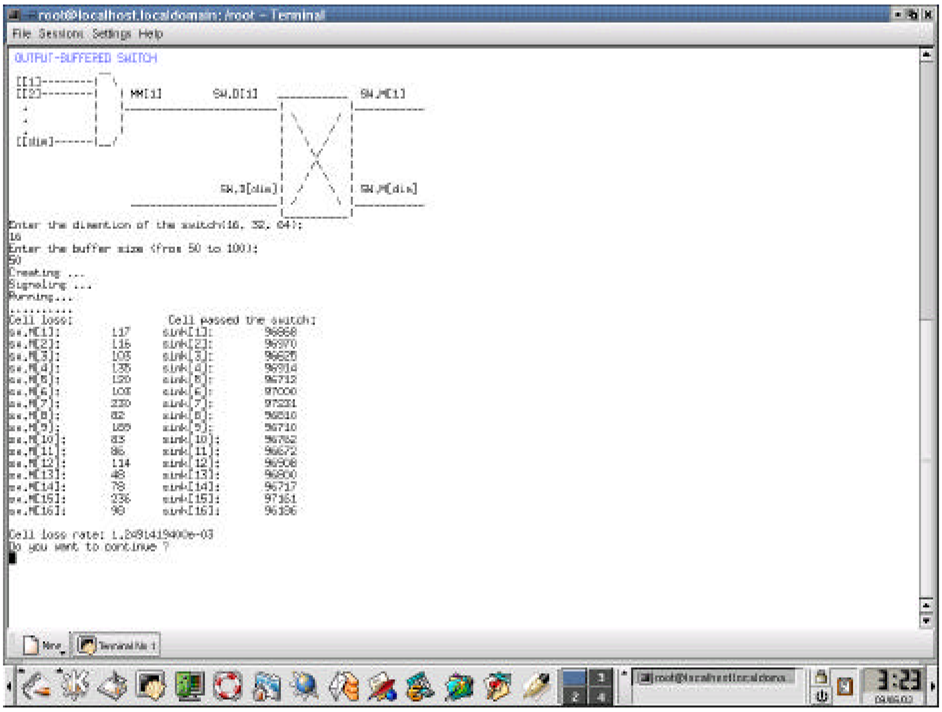

Figure 8: Cell transfer over an switch

6) Cell transfer over two output-buffered switchs

In Figure 9, we represented cell transfer over two 32 x 32 output-buffered switchs, if we sent 3104214 cell we got results such as cell loss : 124, cell pass: 3103220 and cell loss rate : 3.9945699620e-05.

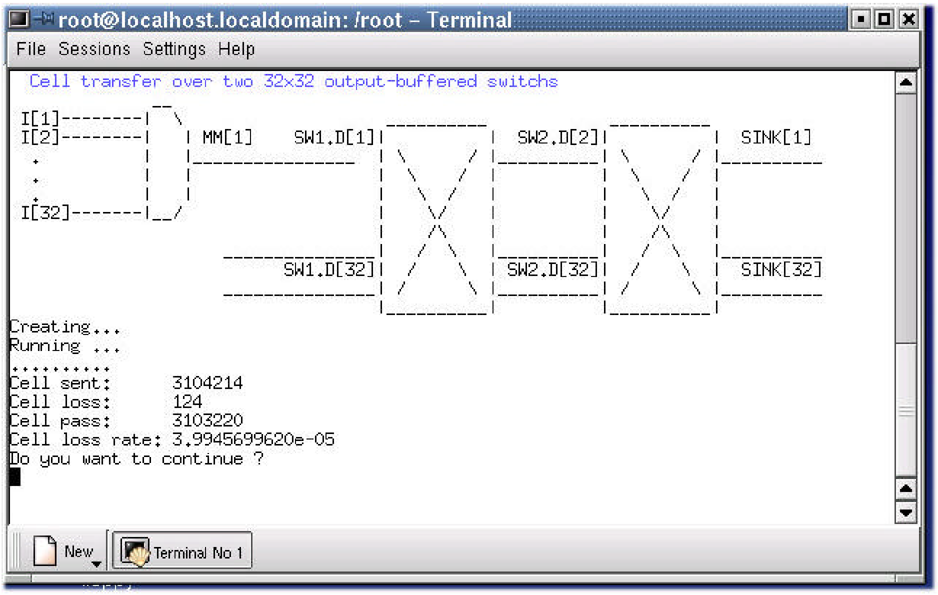

Figure 9: Cell transfer over two output-buffered switchs

7) Cell transfer over several output-buffered switchs

Figure 10 shows the general model of figure 9 which is displayed if we entered 4 switch for input sources.

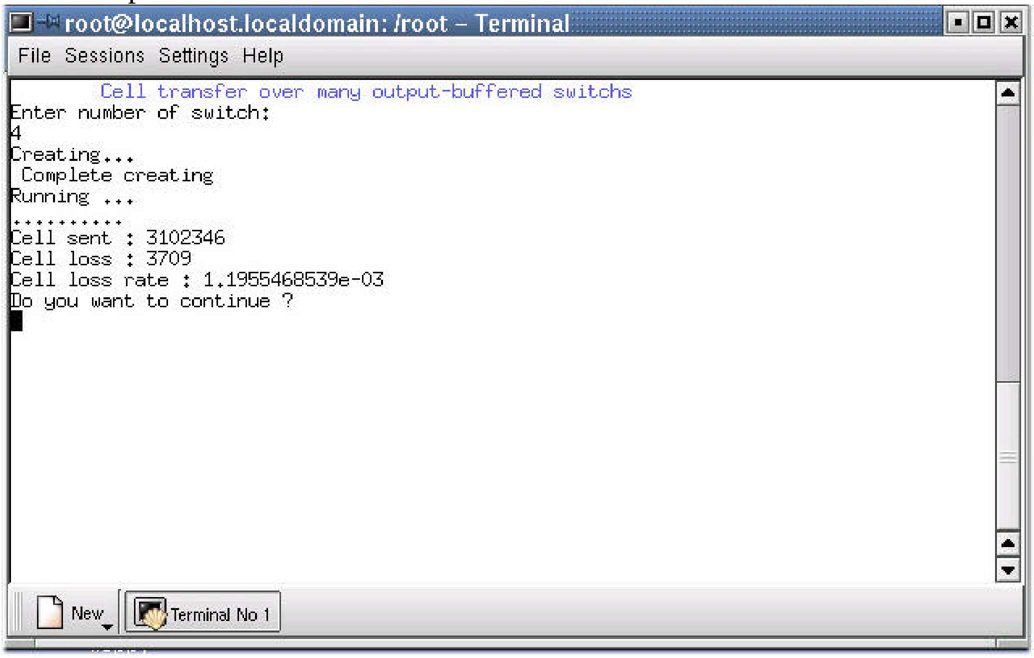

Figure 10 : Cell transfer over several output-buffered switchs

4. Conclusions

In this paper we show six QoS parameters which used to measure the performance of the network for a given connection in ATM network and simulate a various kind of traffic parameters in order to solve many problems such as cell loss, cell transfer delay, etc. using YATS tool. In suggested traffic model, we got the good results as similar as we expected. In our model, we demonstrate the very small average waiting time and show zero cell loss in the multiplexer.

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Sang-Sig Nam was born in 1958 and received the B.S., M.S., and Ph.D. degrees in electronic engineering from Dankook University, Seoul, Korea, in 1981, 1983, and 1999 respectively. He is a Project Leader and Principal Member of the engineering staff at ETRI, which he joined in 1985. He has been engaged in the research and development of digital switching systems such as TDX-1A, 1B, TDX-10 , TDX-10 ISDN, and HANbit ACE ATM & MPLS switching systems. He is a member of the KITE, KICS and KEES of Korea.